Ultra-Broadband AlGaN Amplifier Development

Northrop Grumman Quarterly Program Status Report

Contract number:	N00014-95-C-0171
Program:	Ultra broadband AlGaN amplifier development
Reporting Period:	November 2 1998 - February 2 1999
CDRL:	A001 - Performance and cost report

1. PROGRAM OBJECTIVE:

a) Highly Linear Microwave Amplifier Program (Original Program Phase)

This program report describes work performed under a three year extension of an ongoing effort to develop high linearity microwave amplifiers. Work performed under the initial program phase has now been completed, and the final report submitted. This quarterly report describes selected tasks from the original program phase, including SiC hybrid amplifier fabrication and test, and AlGaN MODFET fabrication and test, to continue the description of these efforts started in the last program report, or because these efforts are continued under the current program phase.

b) Ultra Broadband AlGaN Amplifier Development (Follow-on Program)

The objective of the program extension is to develop and demonstrate an AlGaN MODFET based ultra-broadband (1-18GHz) power amplifier with 3 Watts output power.

To achieve this objective, the program has four major tasks, each with a primary objective:

1. Develop well controlled material deposition procedures, using chemical vapor deposition, for standard and low defect density AlGaN materials growth on high resistivity 6H SiC substrates. These processes will then be used to deposit advanced AlGaN MODFET structures for processing into discrete devices, and fabrication into an ultra-broadband distributed amplifier.
2. Design, model, and fabricate advanced discrete power AlGaN MODFETs, with improved power, efficiency and lifetime to make them suitable for distributed amplifier fabrication. Device performance goals include output power density > 4 W/mm at 10 and 18 GHz, and output power of 1 Watt at 18GHz.
3. Develop and demonstrate MMIC passive components compatible with distributed AlGaN MODFET amplifier use on high resistivity SiC substrates, including Vbd > 50V.
4. Design, fabricate and test an ultra-broadband distributed amplifier using AlGaN MODFETs with 3 Watts output power, 1-18GHz bandwidth.

5. WORK PERFORMED DURING THE CURRENT PROGRAM REPORTING PERIOD:

During the current period, program work was focused in several areas:

1. Modeling and design of AlGaN MODFET structures on SiC substrates.
2. Fabrication of AlGaN MODFETs deposited on SiC substrates using CVD.
3. Assembly and continuing test of the 0.5μm gate length SiC MESFET based hybrid amplifier.
4. The final report for the first program phase was completed and submitted (Highly linear microwave amplifier development).

Details of the work and results in selected areas are described in the following sections.

3. TECHNICAL PROGRESS

3.1 HIGHLY LINEAR MICROWAVE AMPLIFIER PROGRAM: Task R 2.3: SiC MESFET Distributed Amplifier Fabrication and Test

Two distributed amplifiers have been assembled and tested to date. The completed amplifier is shown in Figure 1.

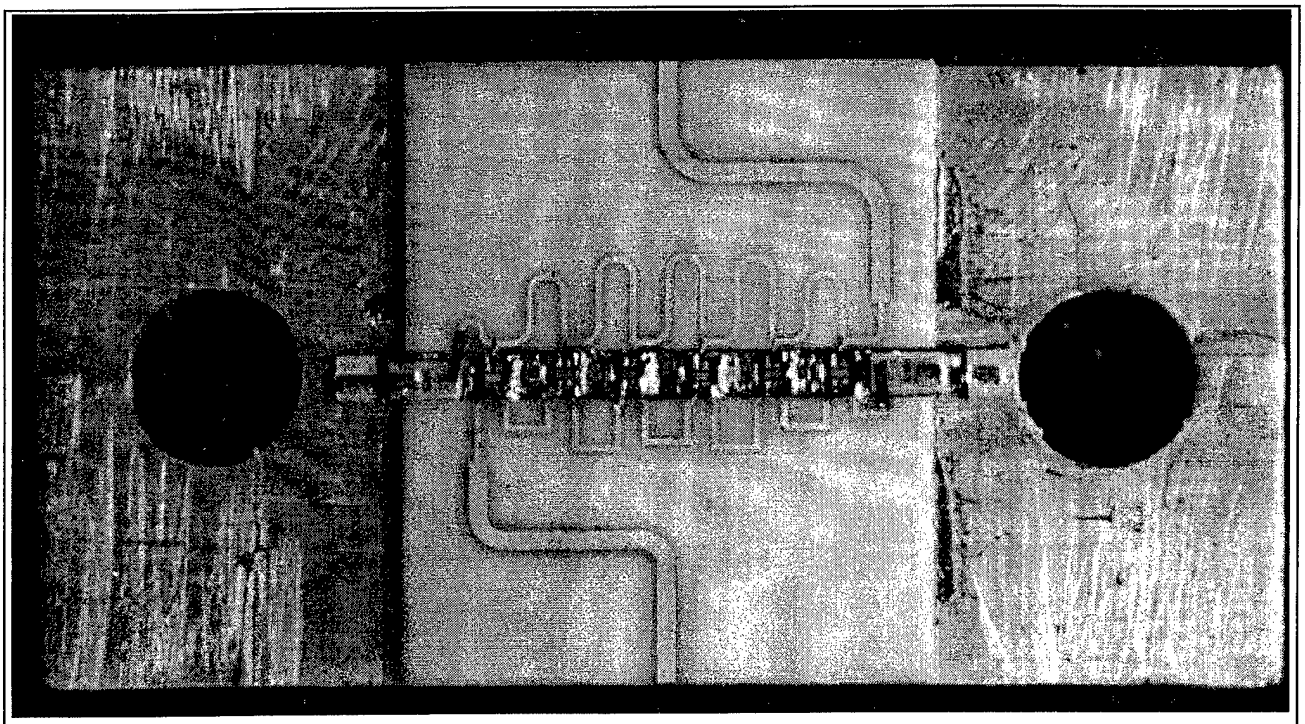
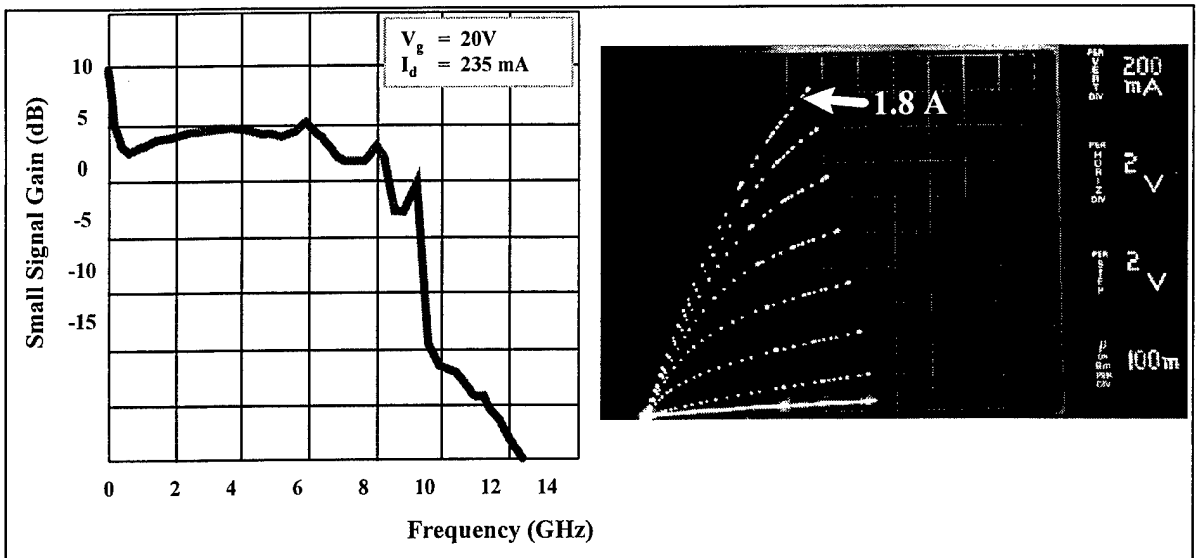


Figure 1: Completed hybrid SiC distributed amplifier

The hybrid amplifier was assembled on an OFHC carrier with 250μm thick polished alumina substrates. Gold microstrip lines were defined using a combination of Cr/Au evaporated metal and gold electroplating to 5μm thickness. Devices and alumina substrates were soldered in place using AuGe eutectic. Bias decoupling was implemented using 18pF MIM chip capacitors in series with the gate and drain line 50Ω termination resistors. Bias current is applied using external commercial bias-T networks. The completed hybrid amplifier assembly was



a) Low Bias Small Signal Characteristics

b) DC Characteristics

Figure 2: Small signal and dc characteristics of the completed SiC distributed amplifier.

tested at DC, small signal and for output power. DC characteristics of the amplifier are shown in Figure 2. The assembled amplifier was placed on our standard microwave test fixture, which provides water cooling. The gold plated brass fixture provides microwave input and output using a pressure contact system. Initially, small signal testing was performed to establish gain and return loss levels. Because bias signals were injected through the internal bias networks in the network analyzer, current was limited to <500mA and voltage to <40V. Also, >40W power dissipation is required when operating at 40V and 50% I_{DSS}. Bias was initially applied to the gate to a voltage sufficient to pinch off the device. The drain voltage was gradually increased to 20V, then the gate voltage was adjusted to allow 200mA drain current and the gain shown in figure 2 was recorded. Under these conditions, the low voltage bias and current results in low amplifier gain. Following this measurement, the drain voltage was increased to the design voltage of 40V by increasing the voltage in 5V steps. When the voltage was increased to 35V, one transistor in the amplifier shorted.

Investigation of the test system showed that this short was indirectly caused by the gate power supply, which contains an auto-ranging feature for measurement of supply current. This auto-ranging selects a resistance for attaining optimum measurement sensitivity. When the range resistance in the supply is too large or too small, the supply output voltage returns to zero, the range resistor is changed and the voltage is reapplied. This process is completed in about 10μsec. When the amplifier drain voltage was increased to 40volts, the gate leakage current increased from <1mA to >1mA. This caused the gate power supply to auto-range the current measurement, setting the voltage to zero, and allowing the full drain current at 35 volts, dissipating over 80 watts of power. This high current and voltage exceeds the device design limit. When the first device "fused" it absorbed nearly all the supply current and limited voltages to less than 5volts.

A second amplifier was assembled. During testing, the auto-ranging features of the power supplies were disabled to prevent the gate voltages that allow high drain current. Measured gain was below that seen with the first amplifier, and significant heating was observed, although the test fixture remained cool. After some preliminary testing, contact problems at the gate line connector again led to high device current levels, and the amplifier failed. A third amplifier is currently being prepared for test.

3.2 ULTRA BROADBAND AlGaN AMPLIFIER DEVELOPMENT: Task 2: AlGaN MODFET Development (Continuation of task R2.2 from the first program phase)

Completion of the first AlGaN MODFET device lot, including MODFET designs with undoped surface layers to

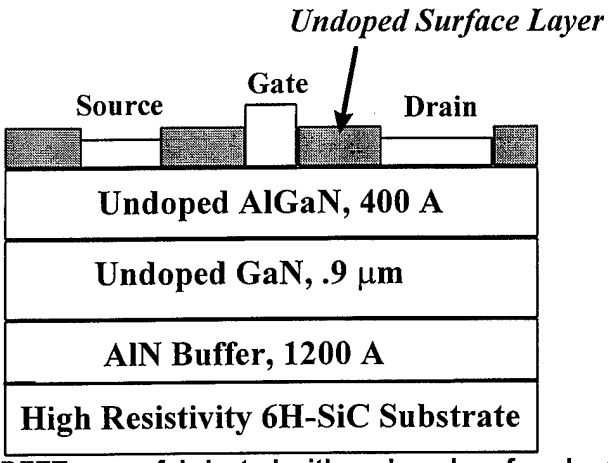


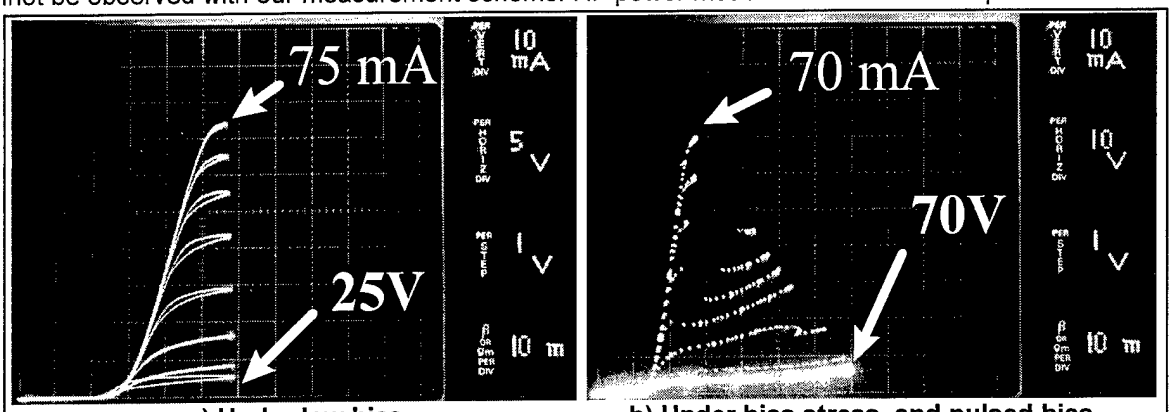
Figure 3: AlGaN MODFETs were fabricated with undoped surface layers and passivation, to evaluate the impact of the AlGaN surface on pulse compression

evaluate their impact on pulse compression, was mentioned in the last quarterly report, and results have been discussed in the final report of the first phase of this program. A brief description of the results obtained for these devices is included in the following paragraph, for completeness and clarity.

MODFET's with Undoped Surface Layers

Figure 3 shows the MODFET structure with an undoped GaN layer near the surface. Dry etching was used to selectively remove this layer under the gate and in the source and drain contact areas. The I-V characteristics of

this structure under low and high voltage bias conditions are shown in figure 4. ***Unlike conventional MODFET's, these devices do not show reduction in drain current after high voltage stressing.*** The observed changes in device behavior with the inclusion of the undoped layer clearly suggest that the surface of GaN MODFET's is responsible for slow trapping effects. However, the present results do not show whether the undoped layer has eliminated the problem or whether it has just modified the slow trapping time constant so that it cannot be observed with our measurement scheme. RF power measurements will be required to confirm this.



a) Under low bias **b) Under bias stress, and pulsed bias**

Figure 4: With the use of the undoped surface layer and passivation, no significant dc pulse compression is observed

Unfortunately RF power measurement is not possible with the present devices which have high contact resistance due to incomplete removal of the undoped layer in the source, drain ohmic contacts. A new processing lot, described in the next paragraph, is now under way. This lot also contains wafers with the undoped layer, to follow-up on these promising initial results.

New Processing Lot

During the current reporting period, processing was initiated on a second lot of AlGaN MODFET structures with undoped layer near the surface for possible elimination of pulse compression. Conventional MODFET structures without the undoped layer, but with a silicon nitride layer as passivation were also included as a reference for comparison. In this second program lot the contact resistance problem was resolved by etching the undoped layer deeper in the contact areas, and annealing the Ti/Al/Ni/Au contact at a higher temperature (900 C versus the 800 C used in the earlier run). In devices with silicon nitride passivation layer, reaction and spreading of the Ti/Al/Ni/Au contact with silicon nitride was eliminated through the use of sintered Ti contacts. Following ohmic contact formation, both types of structure have been processed through Helium implantation for device isolation. Unlike earlier wafers, we observe a residual leakage between isolated areas in the present devices. C-V measurements of the samples indicate that this leakage is due to conduction through either the high resistivity GaN buffer or at the AlN nucleation layer interface. The wafers are presently in the gate fabrication step and any adverse effect of the parasitic leakage will be evaluated following gate deposition.

3.3 ULTRA BROADBAND AlGaN AMPLIFIER DEVELOPMENT: Task 3: MMIC Technology Development

We have initiated work on a high etch rate dry process for the fabrication of through SiC wafer vias. This work is done in cooperation with Prof. Steve Pearton of University of Florida, Gainesville, in their Plasmatherm Inductively Coupled Plasma (ICP) etch system. The etch process uses NF_3 and oxygen as the etch gases for SiC. A key requirement in etching deep vias in SiC is the identification of a mask material that exhibits high etch selectivity over SiC. To evaluate their suitability as a masking medium, we have characterized the etch rates of Al, Ni, Indium Tin Oxide (ITO), and SiC for various process conditions; selected results are shown in Figure 5. From the results obtained to date, Ni appears to be the most promising mask material, but ITO is expected to show improved results with further optimization of the deposition conditions. Under the present etch conditions, creating a 4 mil via in SiC will require about 7 micron thick Nickel masking layer, which can be deposited using an electroplating process

3.4 PLANS FOR THE NEXT PROGRAM REPORTING PERIOD

Processing and testing of the current device lot will be continued during the next reporting period. Device modeling efforts, and MMIC process development will also be continued.

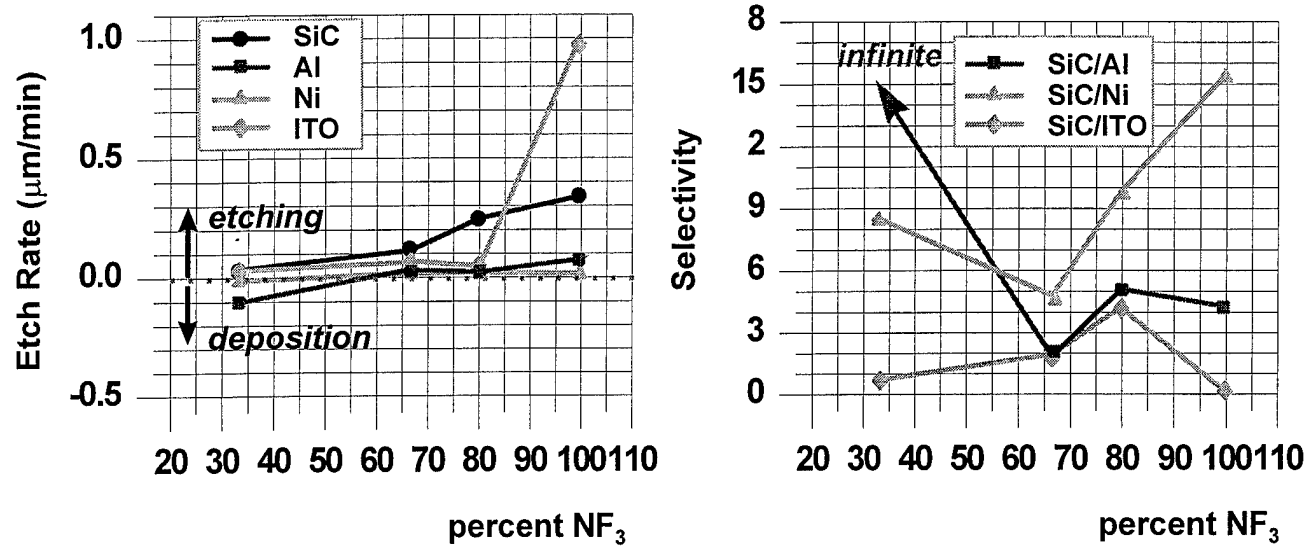
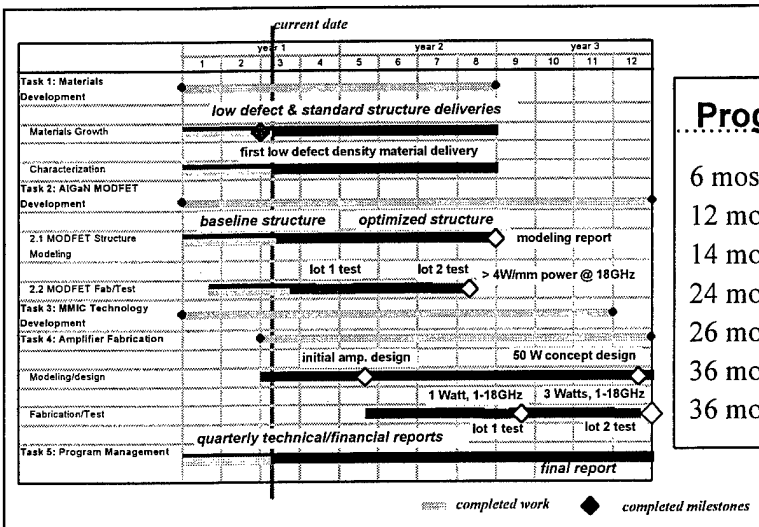


Figure 5: Etch rate and selectivity for masking materials used for dry etching of SiC. (NF3 etching. Total flow NF_3/O_2 = 15 sccm, ICP = 750W, rf power = 250W, pressure = 2 mtorr

4. PROGRAM SCHEDULE AND FINANCIAL PERFORMANCE

Two additional program funding increments, totaling $160K, were received in January. The revised program funding position, and current program spending, are shown in Figure 6. The program schedule, and current status is shown in Figure 7. The current MODFET device lot is expected to be completed and tested during the next quarter.

Evaluation of the initial design of the 1-18GHz amplifier will be initiated during the next reporting period, but detailed amplifier design will be delayed pending testing of the current device lot. The first program milestones (delivery of initial AlGaN MODFET structures grown using the LEO technique) has been completed according to schedule; the material is being characterized at Northrop Grumman.



Program Milestones

6 mos.	Initial Low Defect Material
12 mos.	MODFET with > 4W/mm @ 18GHz
14 mos.	Initial Amplifier Design
24 mos.	Modeling Report
26 mos.	1 Watt, 1-18 GHz Amplifier
36 mos.	3 Watt, 1-18 GHz Amplifier
36 mos.	> 50 Watt, 1-18 GHz Design Concept

Figure 6: Program Schedule status, and program milestones. Low defect density AlGaN MODFET structure growth has been delayed by initial delays in setting up the revised program subcontract with NCSU. This is not expected to adversely impact program progress.

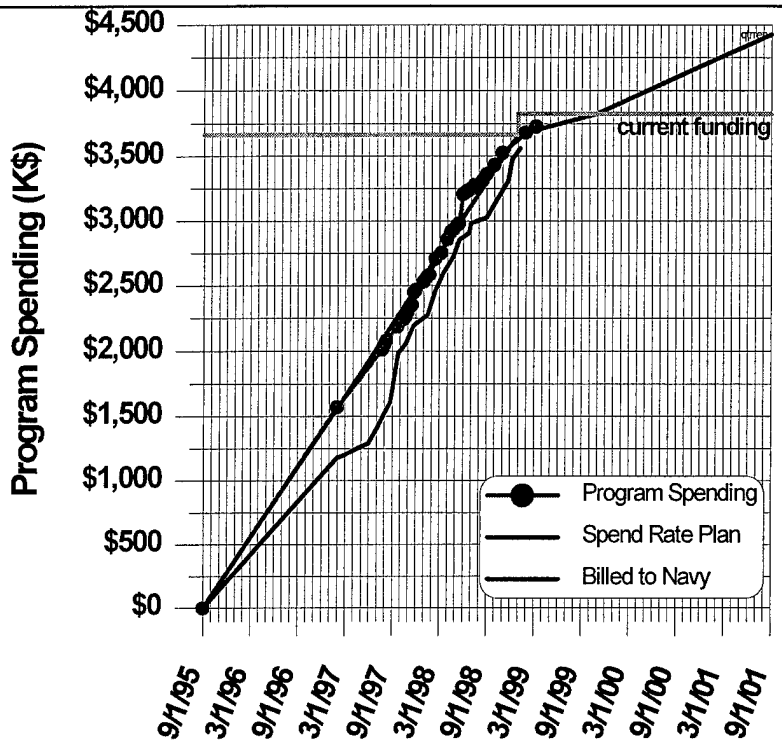


Figure 7: Program spending curve. An additional $160K funding increment has been received. Program spending remains on track, but program efforts will be reduced to reflect the reduced program spend rate plan.